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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,895	01/29/2004	Haruo Nishida	118496	2608

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EXAMINER	
BRITT, CYNTHIA H	
ART UNIT	**PAPER NUMBER**
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/765,895	NISHIDA ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 1/29/04 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

Drawings

Figure 1 A_B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 9-13 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Each of the claims 9-13 merely state: "An integrated circuit comprising: the test circuit as define in claim X; the first macro block; and the second macro block." There is no further limitation on the parent claim.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 9-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Each of the claims 9-13 merely state: "An integrated circuit comprising: the test circuit as define in claim X; the first macro block; and the second macro block." There is no further description of what is being claimed and thus these claims are unclear.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8 and 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,940,414 by Takano et al.

As per claims 1 and 17 Takano et al teach the claimed circuit and method of checking connections between circuit blocks and between each circuit block and external terminals having: a first circuit block and a second circuit block; a first multiplexer having two input terminals connected to an output terminal of the first circuit block and an external input terminal; a control terminal for receiving a first test signal; and an output terminal connected to an input terminal of the second circuit block, for connecting any one of the output terminal of the first circuit block and the external input terminal to the input terminal of the second circuit block; and a second multiplexer having an input terminal connected to the input terminal of the second circuit block; a control terminal for receiving a second test signal; and an output terminal connected to an external output terminal, for connecting or disconnecting the input terminal of the second circuit block to or from the external output terminal; in normal operation mode, the first multiplexer connecting the output terminal of the first circuit block to the input terminal of the second circuit block on the basis of the first test signal, and the second

multiplexer disconnecting the input terminal of the second circuit block from the external output terminal on the basis of the second test signal; in a first test mode for outputting a signal outputted by the first circuit block through the external output terminal, the first multiplexer connecting the output terminal of the first circuit block to the input terminal of the second circuit block on the basis of the first test signal, and the second multiplexer connecting the input terminal of the second circuit block to the external output terminal on the basis of the second test signal; and in a second test mode for inputting a signal inputted to the second circuit block through the external input terminal, the first multiplexer connecting the external input terminal to the input terminal of the second circuit block on the basis of the first test signal, and the second multiplexer disconnecting the input terminal of the second circuit block from the external output terminal on the basis of the second test signal, which comprises: a step of setting a normal operation mode value to the first and second test signals, respectively; a step of inputting the first and second test signals to which the normal operation mode values have been set, to the first and second multiplexers, respectively; a step of obtaining forward direction connection data by tracing a signal path from the output terminal of the first circuit block to the input terminal of the second circuit block via the first multiplexer and another signal path from the output terminal of the first multiplexer to the external output terminal via the second multiplexer; a step of obtaining backward direction connection data by tracing a signal path from the input terminal of the second circuit block to the output terminal of the first circuit block via the first multiplexer and another signal path from the first multiplexer to the external input terminal; and a step of

comparing the forward connection data and the backward connection data with previously-prepared normal connection data, to test the connection relationship in the normal operation mode of the logic circuit. (Abstract Column 3 lines 23-52)

As per claims 2-4, 8, 18, and 19 Takano et al. teach (see FIG 2) "...a multiplexer MUX1 is connected between an output terminal of the circuit block A 21 and an output terminal of a buffer BUF1 connected to an external input terminal EXT11, and an input terminal of the circuit block B 22. Further, another multiplexer MUX2 is connected between an input terminal of the circuit block B 22 and another buffer BFF11 connected to an external output terminal EXT12."(column 4 lines 35-43)

"The multiplexer MUX1 has three NAND circuits NA1, NA2 and NA3, and an inverter INV1. Two input terminals of the NAND circuit NA1 are connected to a signal line 23a connected to the output terminal of the circuit block A 21 and to an output terminal of the inverter INV1 for inputting a test signal TSTB (i.e., an inverted test signal TSTB is inputted to the input terminal thereof). An output terminal of the NAND circuit NA1 is connected to one input terminal of the NAND circuit NA3. Two input terminals of the NAND circuit NA2 are connected to an output terminal of the buffer BUF1 and to an input terminal of the inverter INV1 (i.e., a control terminal to which the test signal TSTB is inputted). An output terminal of the NAND circuit NA2 is connected to the other input terminal of the NAND circuit NA3. Further, an output terminal of the NAND circuit NA3 is connected to the input terminal of the circuit block B 22." (Column 4 lines 44-59 Fig 2)

"The multiplexer MUX2 has three NAND circuits NA11, NA12 and NA13, and an inverter INV11. Two input terminals of the NAND circuit NA11 are connected to a signal line 23b

connected to the input terminal of the circuit block B 22 and to an input terminal of the inverter INV11 (i.e, a control terminal to which another test signal TSTA is inputted). An output terminal of the NAND circuit NA11 is connected to one input terminal of the NAND circuit NA13. Two input terminals of the NAND circuit NA12 are connected to a signal line (to which a signal S1 is outputted by another circuit block (not shown) and then outputted to the outside in the normal operation mode) and to an output terminal of the inverter INV11 (i.e., an inverted test signal TSTA is inputted to the input terminal thereof). An output terminal of the NAND circuit NA12 is connected to the other input terminal of the NAND circuit NA13. Further, an output terminal of the NAND circuit NA13 is connected to an external output terminal EXT12 via another buffer BUF11. " (Column 4 line 60 through column 5 line 11)

As per claims 5-7 and 19-20, Takano et al teach (Fig 4 step 103) "...the signal lines between the input/output terminals of each circuit block and the input/output terminals or the external input/output terminals of other circuit block connected thereto are traced in sequence to check whether these signal lines are activated or not. In other words, the correct circuit connection relationship in the normal operation mode is inspected. In more detail, all the input/output terminals of all the circuit blocks are inspected terminal by terminal as to whether the signal lines between two terminals have been activated or not in sequence. In the case of the logic circuit shown in FIG. 2, for instance, the signal line from the output terminal of the circuit block A 21 to the input terminal of the circuit block B 22 is inspected as to whether activated or not. In the above step 102, since the two test signals TSTA and TSTB are both set to the logic

level [0], when these logic values [0] are inputted to the two multiplexers MUX1 and MUX2 respectively, the connection conditions of the two multiplexers MUX1 and MUX2 can be set. Under these connection conditions, the signal lines are traced in sequence along the path from the output terminal of the circuit block A 21 to the input terminal of the circuit block B 22 via the multiplexer MUX1 (i.e., two NAND circuits NA1 and NA3), to inspect whether this path is activated or not." (Column 8 lines 7-31)

"Here, the above-mentioned path trace processing is a forward direction processing for tracing the signal path in the forward signal path direction from the input side to the output side (in the same direction that the signal is transmitted). After this forward direction processing, a backward direction processing for tracing the signal path in the backward signal path direction from the output side to the input side (in a direction opposite to that the signal is transmitted). That is, the signal line from the input terminal of the circuit block B 22 to the output terminal of the circuit block A 21 via the multiplexer MUX1 (i.e., the NAND circuits NA3 and NA1) is inspected as to whether activated or not. For instance, when the input terminal of the circuit block B 22 is at the logic level [0], it can be understood that the two input terminals of the NAND circuit NA3 are both at the logic level [1]. Further, since the logic level [1] is given to one input terminal of the NAND circuit NA1 via the inverter INV1, it can be understood that the output terminal of the circuit block A 21 is at the logic level [0]. Therefore, under these conditions, it can be clarified that the path from the input terminal of the circuit block B 22 to the output terminal of the circuit block A 21 is activated. In the same way, since the test signal TSTB of the logic level [0] is inputted to one input terminal of the NAND circuit NA2, it

can be understood that the external input/output terminal EXT11 and the NAND circuit NA2 are disconnected from each other, irrespective of the logic level of the external input/output terminal EXT11 (i.e. the other input terminal of the NAND circuit NA2). During the path-trace processing as described above, the connection data in the normal operation mode are stored in the normal operation connection data memory section 4." (Column 8 lines 32-63)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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This patent teaches that at every path connecting the output terminal of a megacell block and the input terminal of random block provided are the first scan cell, the first multiplexer selecting one of the output of the megacell block or the output of the first scan cell based on the first test mode signal and sending to the input terminal of the random block and the second multiplexer selecting the output of the first multiplexer based on the second test mode signal and sending to the external terminal of the integrated circuit device. Also at every path connecting the output terminal of the random block and the input terminal of the megacell block, provided are the third multiplexer selecting one of the output of the random block or the test data input from the external terminal of the integrated circuit device and sending to the input terminal of

the megacell block based on the second test mode signal and the second scan cell receiving the output of the third multiplexer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt
Primary Examiner
Art Unit 2138